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RPC Trigger Status and Plans

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RPC Trigger status

Link System

- Design delivered for production
- Contract details being discussed
- http://pccms9.igf.fuw.edu.pl/users/tb/CMS/Link_System/

Splitter

- In production

Trigger Board

- PPP validated, final routing in progress
- http://pccms9.igf.fuw.edu.pl/users/tb/CMS/Trigger_System/

Sorter

- Design finished

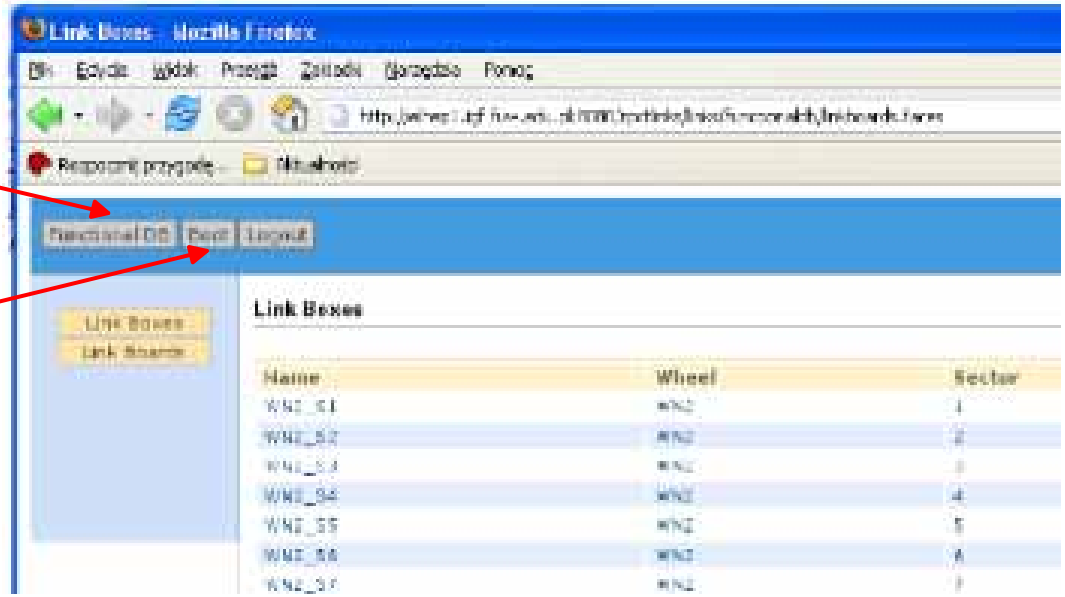
Link Boxes database

- works together with RPCTrigger database

- delivers all data needed to configure the LBB system
  - FPGA configuration files
  - I2C addresses
  - missing RPC strips (construction)
  - masks on broken (noisy) strips
  - link configuration, etc

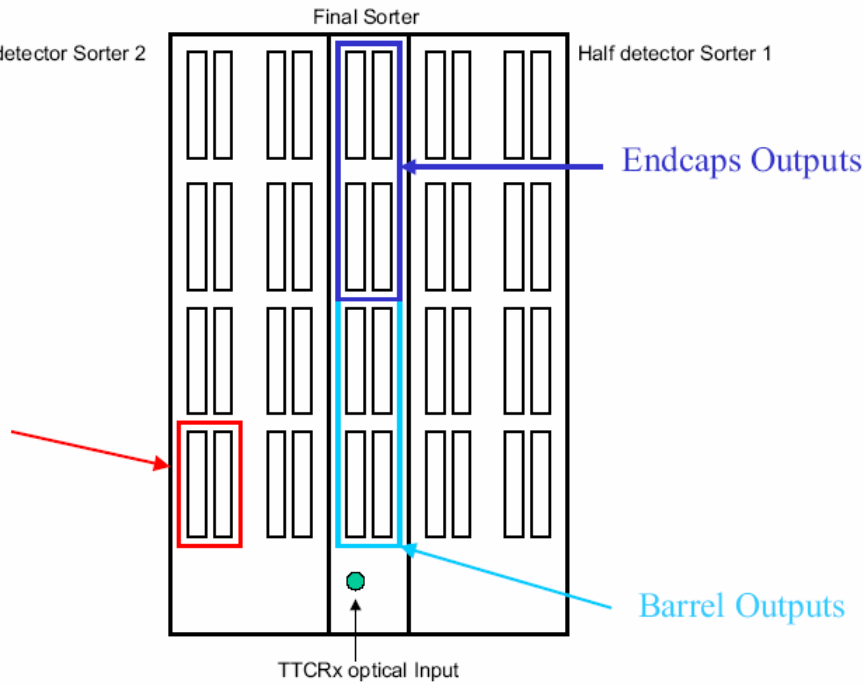
Functional DB (cables, boards, etc) area

Download area



RPC SORTER Project

Sorter boards structure - Bari

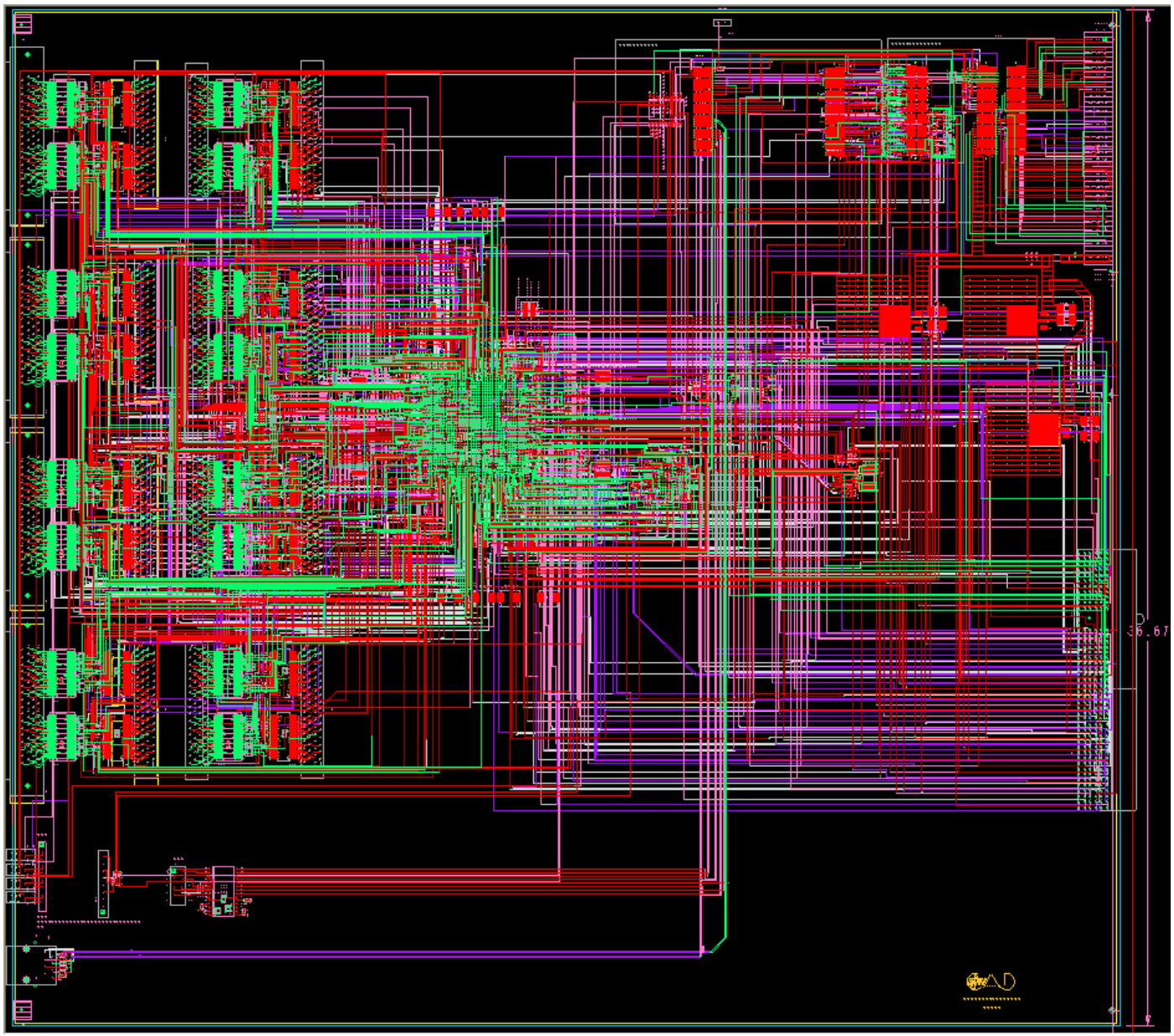


Giuseppe de Robertis fecit

- PCB layout of Half Sorter Board, submitted for the construction:
  - board delivered with mounted components and ready for testing end of March
- Final Sorter Board layout ready for revision:
  - submission for contruction after Easter
- Sorter Backplane layout design starting very soon

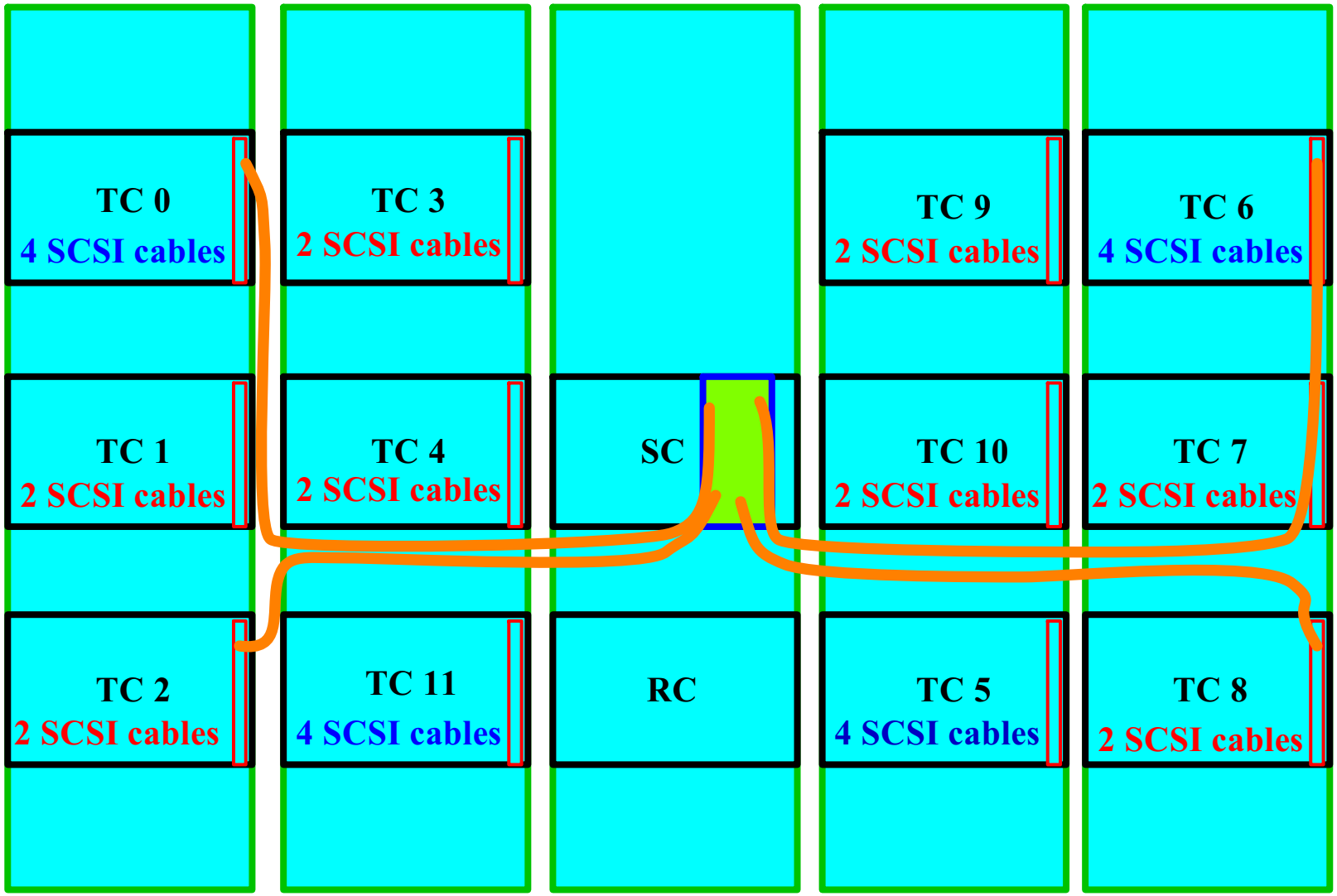
RPC SORTER Project

Layout of the “Half Sorter”



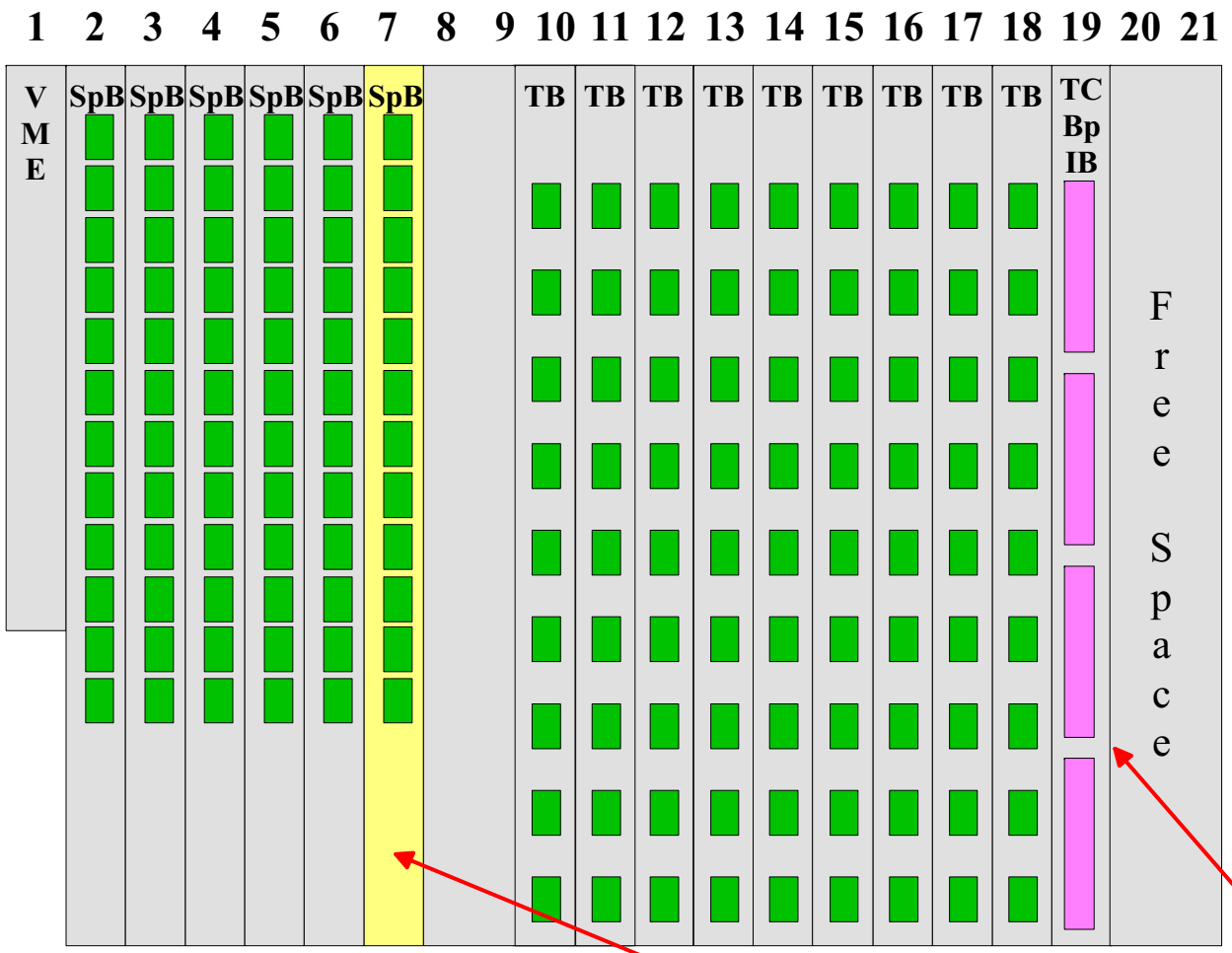
Trigger Crate

TC and SC Crates

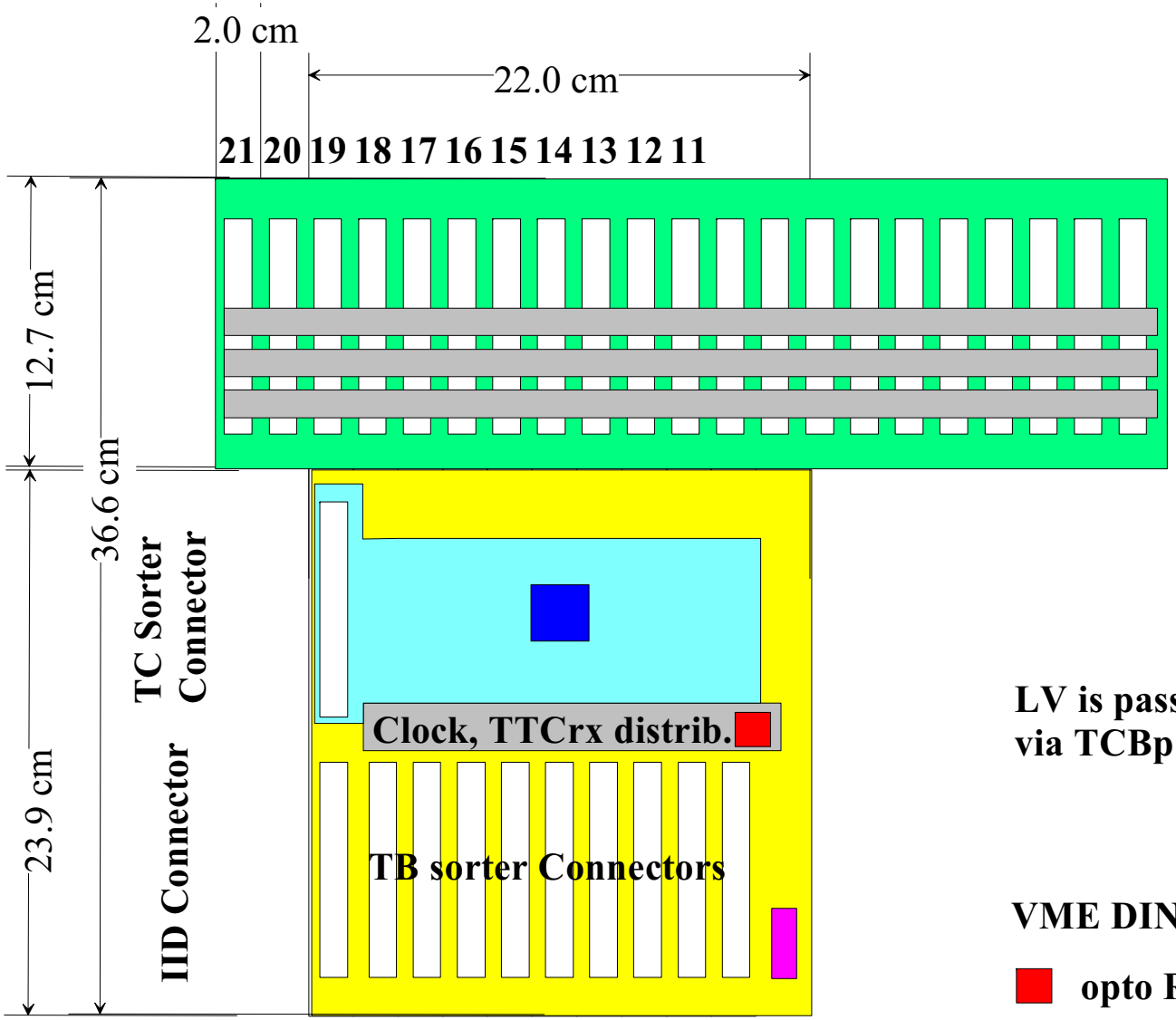


Cables length(max) => 1m + 2*.5m + .5m = 2.5m
total number of SCSI cables => 32 cables

Trigger Crate - front view



Trigger Crate Backplane



LV is passing to TCBp via TCBp J1, J2

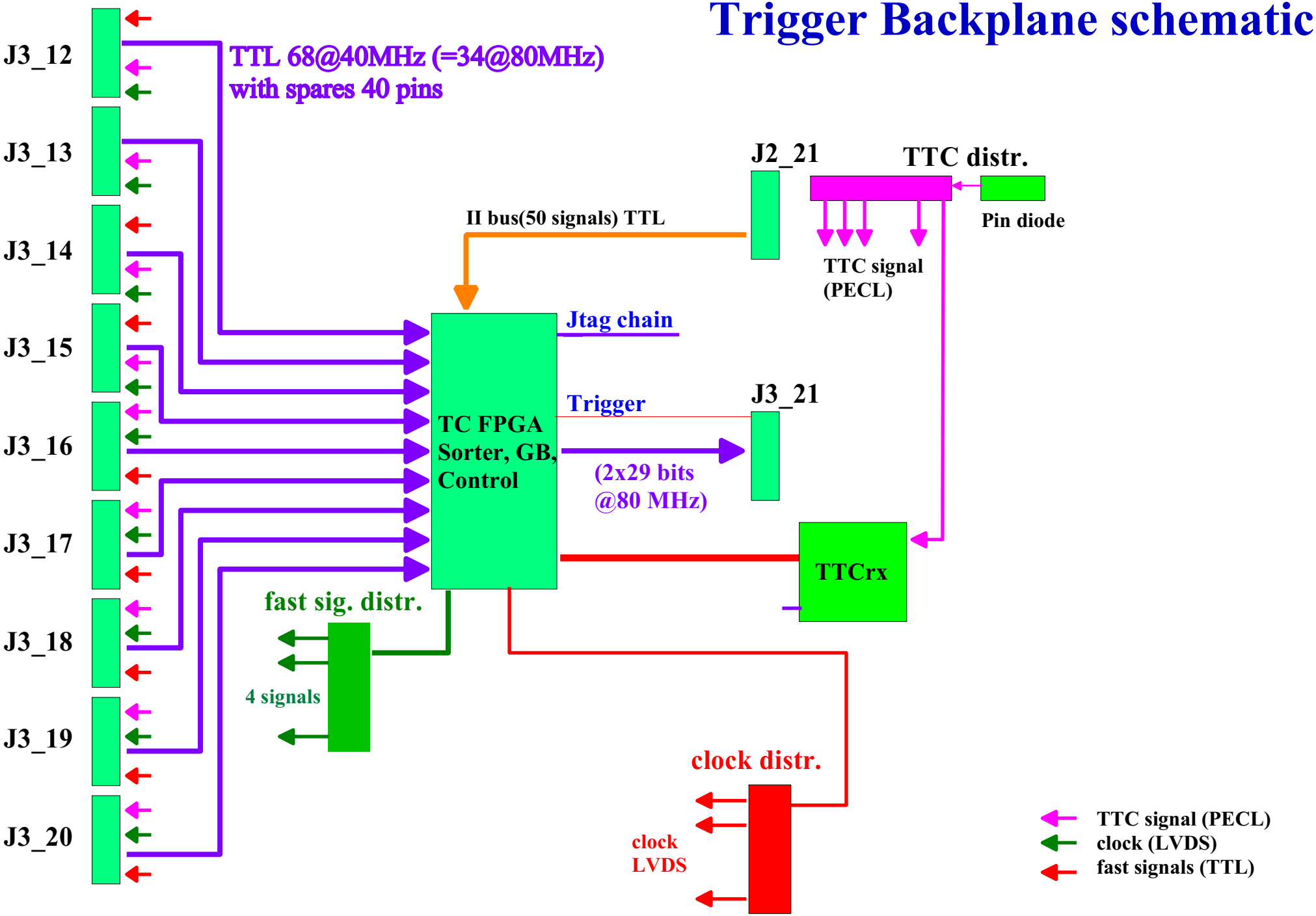
VME DIN 41612 160pin

opto Receiver TTCrx

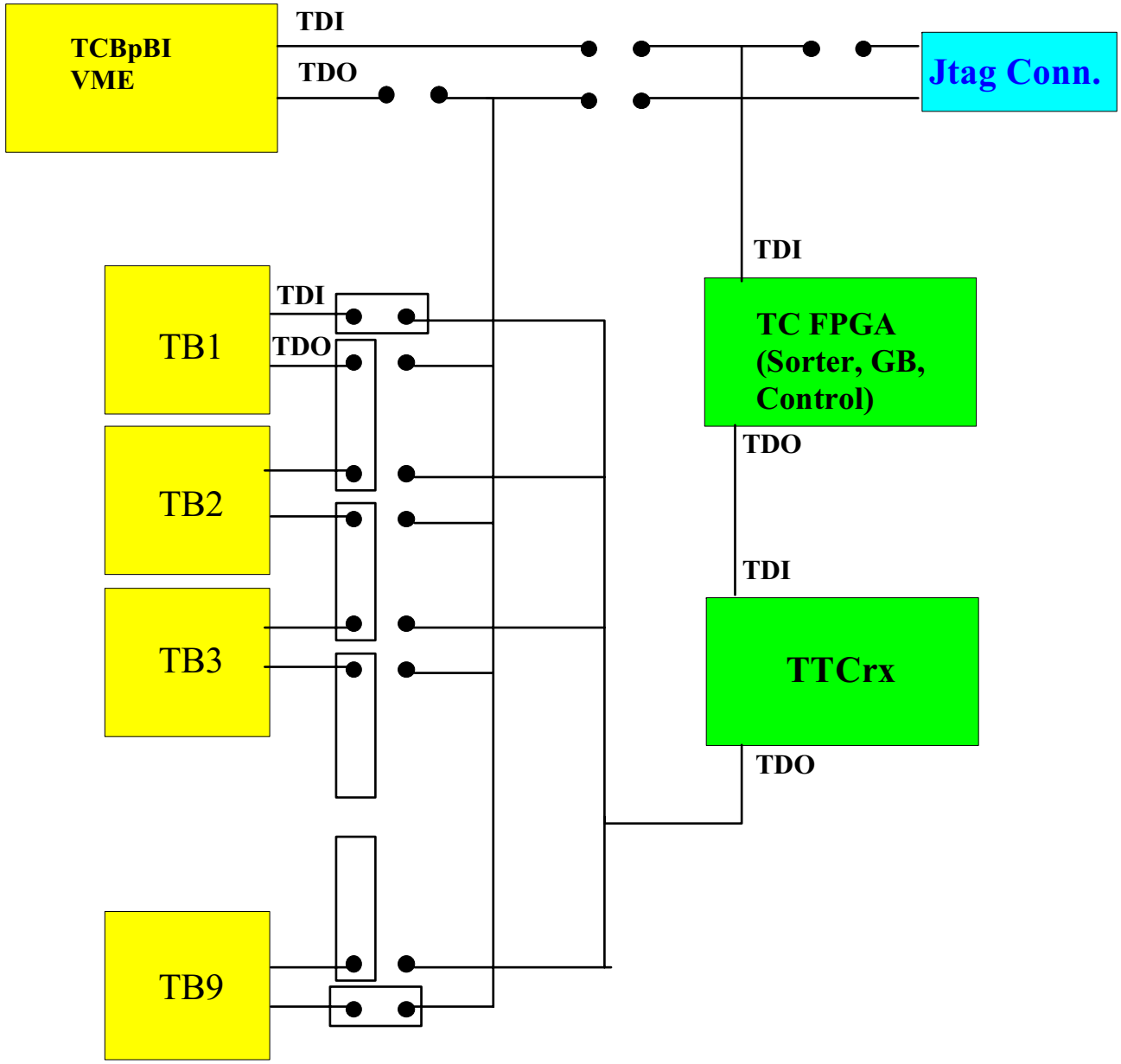
LV connector

Trigger Backplane

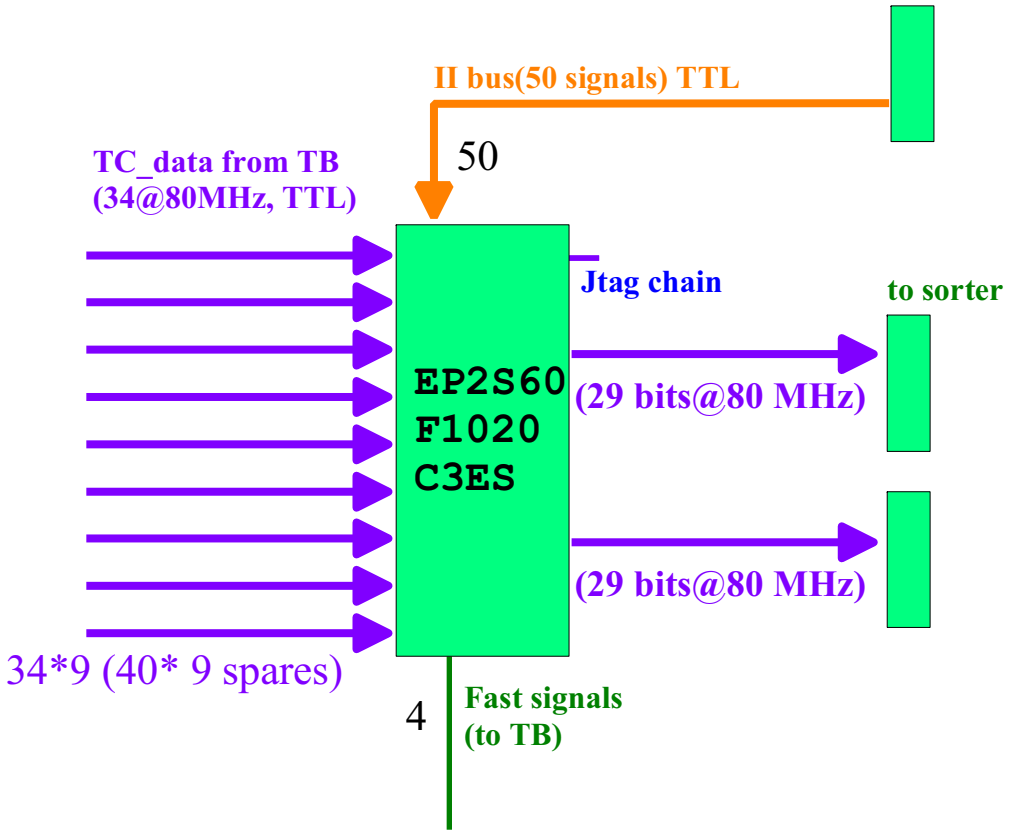
Trigger Backplane schematic



Jtag chain in TC



Trigger Backplane FPGA



34*9+42+50+8+18=306+118=424

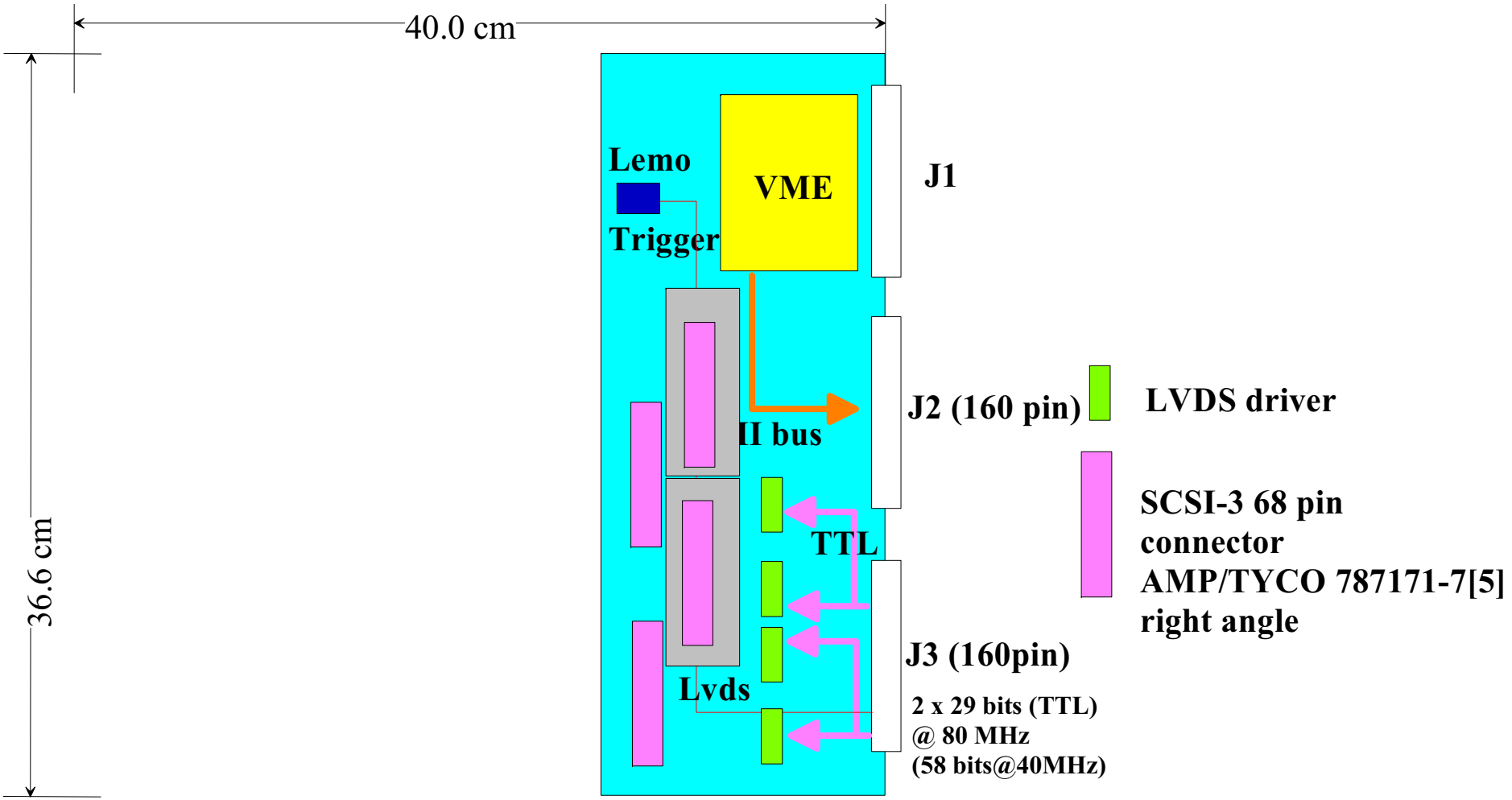
40*9+58+50+4=360+112=472 (with spare bits from TB)

Fitter Summary	
Fitter Status	Successful - Tue Jan 11 16:55:48 2005
Quartus II Version	4.1 Build 207 08/26/2004 SP 1 SJ Full Version
Revision Name	m_tc_gb
Top-level Entity Name	m_tc_gb
Family	Stratix II
Device	EP2S60F1020C3ES
Timing Models	Production
Total ALUTs	24,167 / 48,352 (49 %)
Total pins	439 / 719 (61 %)
Total memory bits	0 / 2,544,192 (0 %)
DSP block 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 12 (0 %)
Total DLLs	0 / 2 (0 %)

Trigger Backplane Interface Board

- delivers VME cotrol to backplane
- makes sorter interface

Backplane Interface Board

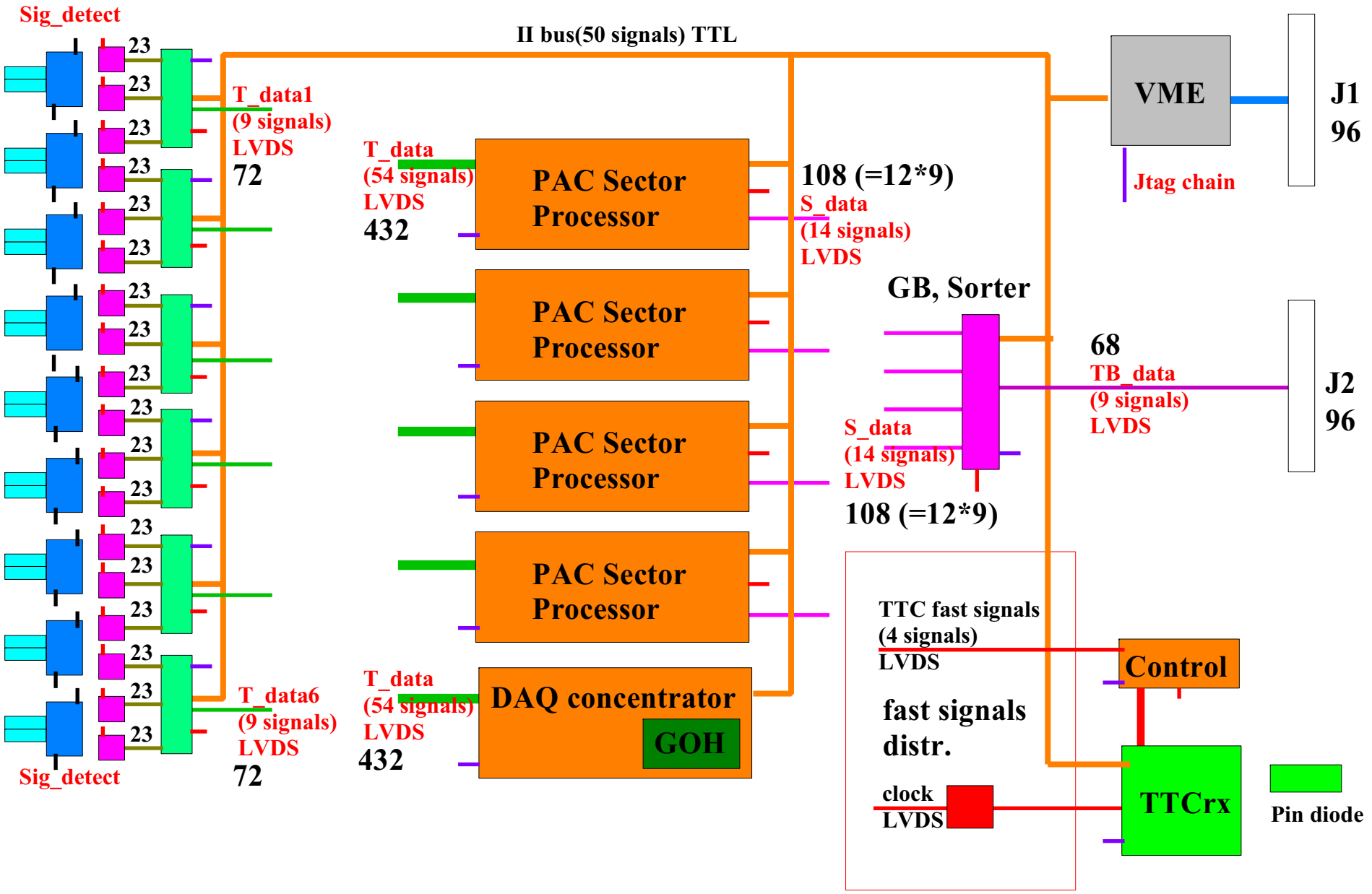


SCSI connectors - sorter signals

	Connector A						Connector B			
	Pin # (P)	Pin # (N)	Signal (L)	Signal (H)			Pin # (P)	Pin # (N)	Signal (L)	Signal (H)
	1	35	TMA (0)	TMA (1)			1	35	TMB (0)	TMB (1)
0	2	36	BCN0	M0_Eta_Add<2>	28	28	2	36	BCN0	M2_Eta_Add<2>
1	3	37	BCN<0>	M0_Eta_Add<3>	29	29	3	37	BCN<0>	M2_Eta_Add<3>
2	4	38	BCN<1>	M0_Eta_Add<4>	30	30	4	38	BCN<1>	M2_Eta_Add<4>
3	5	39	BCN<2>	M0_Eta_Add<5>	31	31	5	39	BCN<2>	M2_Eta_Add<5>
4	6	40	BCN<3>	M0_Gb<0>	32	32	6	40	BCN<3>	M2_Gb<0>
5	7	41	BCN<4>	M0_Gb<1>	33	33	7	41	BCN<4>	M2_Gb<1>
6	8	42	BCN<5>	M1_Sign	34	34	8	42	BCN<5>	M3_Sign
7	9	43	BCN<6>	M1_Quality<0>	35	35	9	43	BCN<6>	M3_Quality<0>
8	10	44	BCN<7>	M1_Quality<1>	36	36	10	44	BCN<7>	M3_Quality<1>
9	11	45	Checksum<0>	M1_Quality<2>	37	37	11	45	Checksum<0>	M3_Quality<2>
10	12	46	Checksum<1>	M1_Code<0>	38	38	12	46	Checksum<1>	M3_Code<0>
11	13	47	Checksum<2>	M1_Code<1>	39	39	13	47	Checksum<2>	M3_Code<1>
12	14	48	Checksum<3>	M1_Code<2>	40	40	14	48	Checksum<3>	M3_Code<2>
	15	49	GND	GND			15	49	GND	GND
	16	50	GND	GND			16	50	GND	GND
	17	51	GND	GND			17	51	GND	GND
	18	52	GND	GND			18	52	GND	GND
	19	53	GND	GND			19	53	GND	GND
13	20	54	M0_Sign	M1_Code<3>	41	41	20	54	M2_Sign	M3_Code<3>
14	21	55	M0_Quality<0>	M1_Code<4>	42	42	21	55	M2_Quality<0>	M3_Code<4>
15	22	56	M0_Quality<1>	M1_Phi_Add<0>	43	43	22	56	M2_Quality<1>	M3_Phi_Add<0>
16	23	57	M0_Quality<2>	M1_Phi_Add<1>	44	44	23	57	M2_Quality<2>	M3_Phi_Add<1>
17	24	58	M0_Code<0>	M1_Phi_Add<2>	45	45	24	58	M2_Code<0>	M3_Phi_Add<2>
18	25	59	M0_Code<1>	M1_Phi_Add<3>	46	46	25	59	M2_Code<1>	M3_Phi_Add<3>
19	26	60	M0_Code<2>	M1_Eta_Add<0>	47	47	26	60	M2_Code<2>	M3_Eta_Add<0>
20	27	61	M0_Code<3>	M1_Eta_Add<1>	48	48	27	61	M2_Code<3>	M3_Eta_Add<1>
21	28	62	M0_Code<4>	M1_Eta_Add<2>	49	49	28	62	M2_Code<4>	M3_Eta_Add<2>
22	29	63	M0_Phi_Add<0>	M1_Eta_Add<3>	50	50	29	63	M2_Phi_Add<0>	M3_Eta_Add<3>
23	30	64	M0_Phi_Add<1>	M1_Eta_Add<4>	51	51	30	64	M2_Phi_Add<1>	M3_Eta_Add<4>
24	31	65	M0_Phi_Add<2>	M1_Eta_Add<5>	52	52	31	65	M2_Phi_Add<2>	M3_Eta_Add<5>
25	32	66	M0_Phi_Add<3>	M1_Gb<0>	53	53	32	66	M2_Phi_Add<3>	M3_Gb<0>
26	33	67	M0_Eta_Add<0>	M1_Gb<1>	54	54	33	67	M2_Eta_Add<0>	M3_Gb<1>
27	34	68	M0_Eta_Add<1>	Unused	55		34	68	M2_Eta_Add<1>	Unused

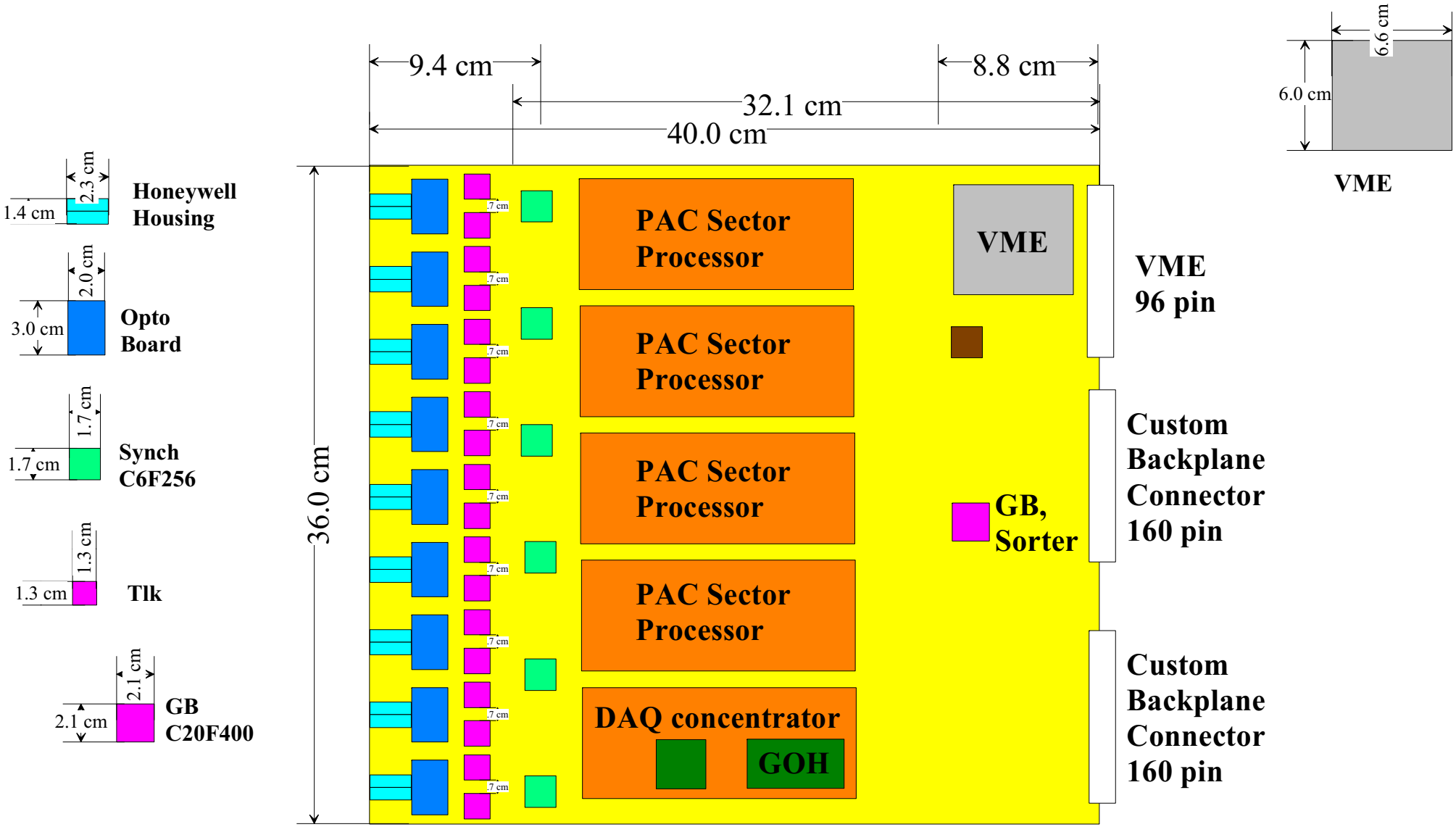
Trigger Board

Trigger Board schematics

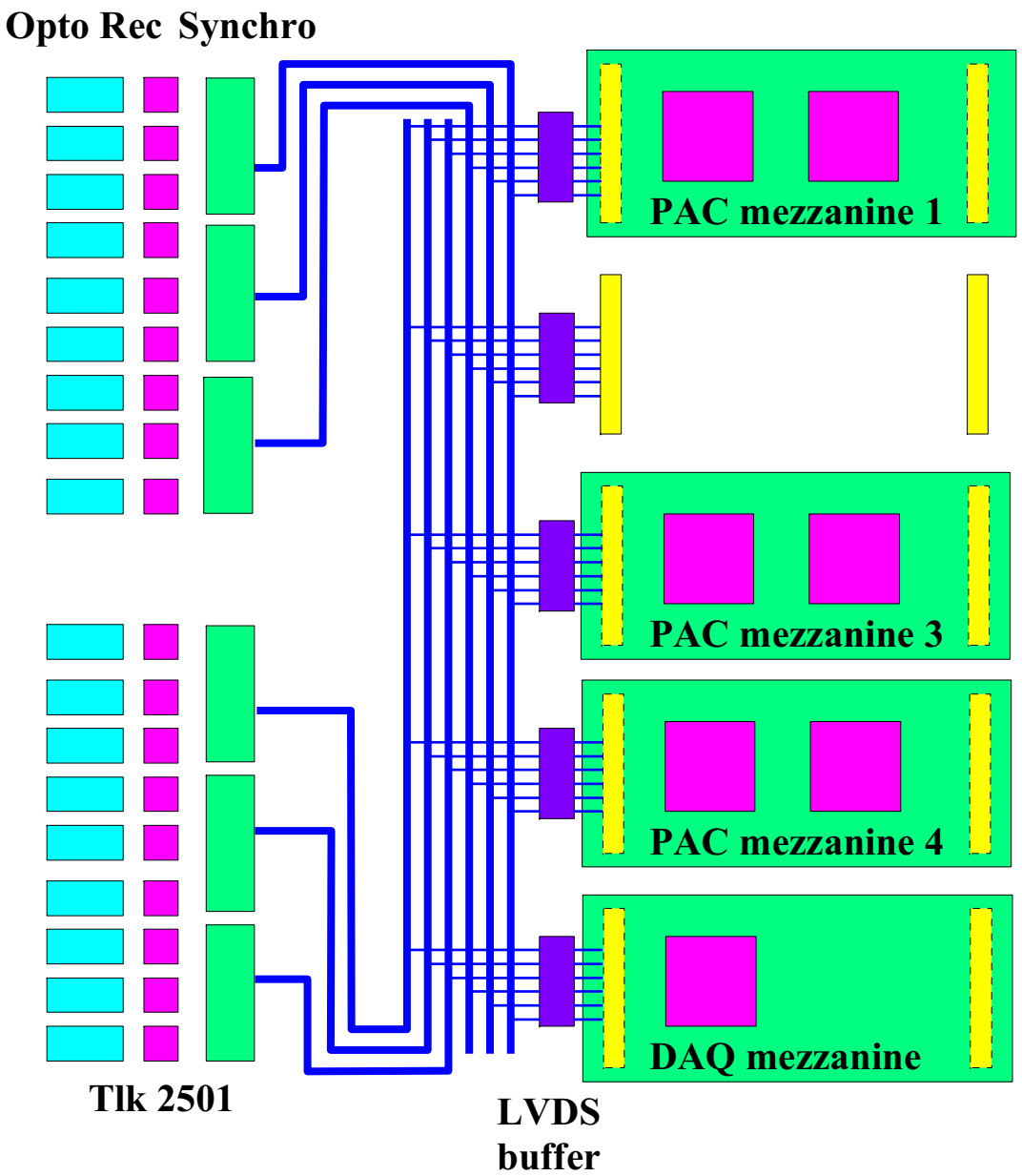


All TB furnishes only 4 highest momentum muons
4 highest momentum muons for endcap and barrel are selected at backplane or final sorter at basis of it eta address

Trigger Board layout



Trigger Board



Optical receiver tests done (see next page)

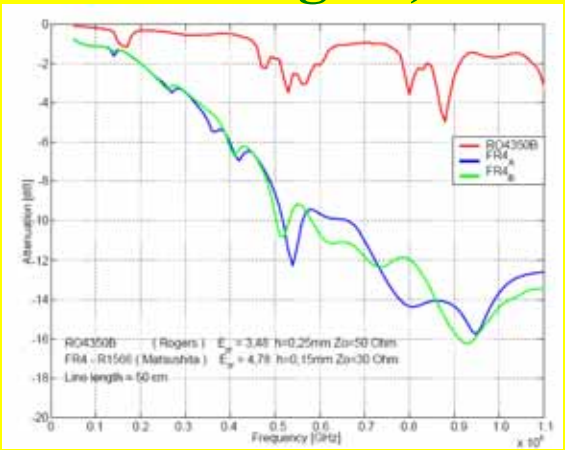
Board transmission study done

Board transmission test, measurements done (see next page)

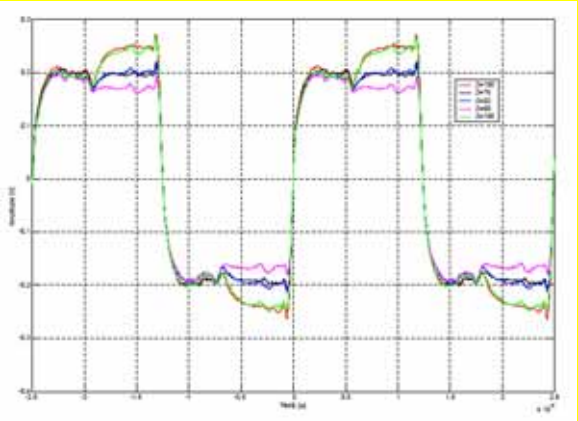
TB board routing starts

Trigger Board prototype tests, measurements

PCB material tests (standard FR4 - ceramic Rogers)



Signal termination study



Eye diagram of optical signal

Eye diagram of board transmission signal

...

and many other

Result - all 54 (point to 5 points) 320MHz LVDS lines work correctly!
TB preproduction board ready to routing!

Under construction production prototypes:

Trigger Board
Trigger Backplane
Trigger Backplane Interface Board

Commissioning & Cosmic Challenge

Link System preproduction:
4 Link Crates (~60 Link Boards) to be used for

- **Integration in B 904** - starting ~May 2005
  - integrate RPC Trigger full chain
  - integrate with RPC DCS
  - integrate with CSC RAT - sychronisation procedures!
  - integrate with Global Muon Trigger

- **RPC commissioning**
  - 1 Link Crate content for RB + 1 for RE

- **Cosmic Challenge**
  - 60^{o} sector of RB1-4 and RE1/2,3

RPC Trigger simulation

New version committed to ORCA repository:

- **all RPC planes (up to 6) used**
  - changed meaning of quality bits
- **PAC ASIC replaced by FPGA**
  - sophisticated tricks needed to fit all patterns into FPGA
  - simple notion of “pattern” no longer valid
- **up-to-date Sorter and Ghost Buster algorithms**
- **detailed layout of the Link System from Data Base**

Official release pending:

- **finalizing PAC VHDL**
  - generation of final “patterns”
- **implementing realistic RPC performance in digitisation**
  - RPC group will take care

RPC Trigger Milestones

	item	milestone	date	comment
RPC	LinkBoard	Production start	Jan-05	Delayed Mar-05
RPC	TriggerBd	PPP done	Done	
RPC	Sorter	Design done	Jan-05	Done
RPC	R/O Board	PPP done	-	Included on TB
RPC	Crate	Proto done	May-05	
RPC	LinkBoard	Production done	Dec-05	
RPC	TriggerBd	Production start	Feb-05	Delayed Aug-05
RPC	Splitter	Production start	Done	
RPC	System	System test (2 crates)	May-05	
RPC	TriggerBd	Produced & tested	Dec-05	
RPC	R/O Board	Produced & tested	-	Included on TB
RPC	Crate	Produced & tested	Dec-05	
RPC	Sorter	Produced & tested	Dec-05	